Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.019”**

**.030”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” min.**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: MG DIE SIZE .019” X .030” DATE: 6/22/23**

**MFG: Vishay THICKNESS .010” P/N: CBA3750CLAHWS**

**DG 10.1.2**

#### Rev B, 7/19/02